Design for Verification:
reduce, reuse, recycle

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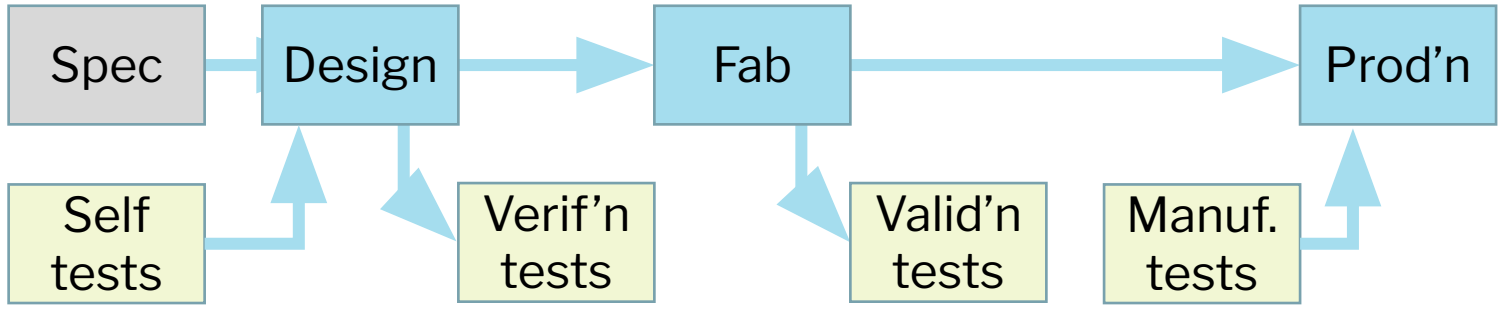
Introduction



During IC development, many tests are written, each in different language

- Self-test in system less process reliability, more FuSa requirements
- Verification more, larger IP blocks (+3rd party), more process corners
- Validate 1st silicon more benchtop equipment, more Eng. samples
- Manufacturing test fewer test engineers, less access to designers

Opportunity to reduce time to create tests, and reuse them

- Use a simple, flexible test description language, linked to DfV

High-level ‘test’ languages

standard terms

Universal Verification Methodology (UVM

Portable Test and Stimulus Standard (PSS

- Built on SystemVerilog, not very intuitive
- Digital, minimal analog
- Don’t guide HW generation or DfV
- Not usable beyond simulation

IEEE 1687 “IJTAG”

- Widely used – guides DfT and test generation
- Only synchronous digital

UVM

```
typedef uvm_sequence_library atb_virt_protocol;
class ate_atb_seq extends ate_basic_virt_pdl_seq;
  `uvm_object_utils(ate_atb_seq)
  `uvm_declare_p_sequencer(tb_top_virt_sequencer)
virtual task atb_select_measure(
    string reg_name, int i2c_data, real i2c_period,
    real nominal, real tolerance, offset, V_pin, I_pin,
    string pin);
  real high_limit, Value, Curr_value;
  high_limit = nominal * (1.0 + tolerance);
  inote = "Best practice TE: put ATB to neutral";
  ate_transparent_comment(inote);
```

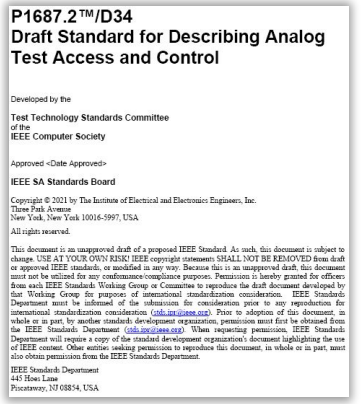
[Zivkovic ETS’22]

PSS

```
component uart_c {
  import dma_xfer_pkg::*;
  resource uart_r { ... };
  pool [1] uart_r uart_p;
  bin
  action read_in_a {
    output data_stream_s data; // via import
    lock uart_r myuart;
    constraint c1 {data.size % 4 == 0;}
  };
```

[Accelera DVCon’20]

A/MS DfT and testing


P1687.2™/D34
Draft Standard for Describing Analog Test Access and Control

Developed by the

Test Technology Standards Committee
of the
IEEE Computer Society

Approved <Date Approved>

IEEE SA Standards Board

EDA for analog DfT and test generation is far behind digital

- Digital automated scan insertion and test generation much higher quality ICs
- Most ICs contain analog, esp. automotive limits quality & TTM improvement

Since 2014, experts developing language to describe test access and control

- 6 now 35, from 20 companies: AMD .. Cohu .. Intel .. NXP .. Siemens .. Teradyne …
- IEEE P1687.2 is analog extension to 1687
  - Instrument Connectivity Language (ICL) – describes module port specifications, connections
  - Procedural Description Language (PDL) – describes test requirements, flow, intent

Analog ICL

```
Module ADC {
  DataInPort   setup[7:0];
  DataInPort   en1;
  AnalogPort   ADCin {Frequency=0:3k; TheveninResistance=1k;
                      ConnectEnable en1;}
  ClockPort    clkin;
  AnalogPort   clkin {Period 100n:300n:1u; RealTimeControl yes;}
  Instance x1 Of gainblock {
    Port       in = ADCin;
    InputPort  En = en1;
  }
}
```

70 properties

Analog PDL

adjustable cycle time

```
set vddmax 3.3
iForceVoltage vddin $vddmax {CurrentDC 0:300m}
iApply
iWrite fastcount 1
iApply
iForceVoltage initData[1] DIGITAL {Data {01110101}; Period=10n;}
iForceVoltage analogIn 1.6 {Frequency {21k, 70k}; VoltageAmplitude {100m, 55m};}
iSet vouts MeasureVoltage analogOut {SampleFrequency 93.2k; Samples 1024;}
iApply -coherent {analogIn analogOut}
iSet vmax iMath Max(vouts)/0.1
iTest {vmax} {TestLimits 29.9m:30.1m; TestName VoutGain; TestID test1;}
iIf {vmax < 0.5} {
  iForceVoltage vddin 0 {PWL {0 $vddmax, 10m 3.0};}
  iSet v2 iMeasureVoltage pin2
  iApply
  }
```

50 properties

90 functions

Next steps

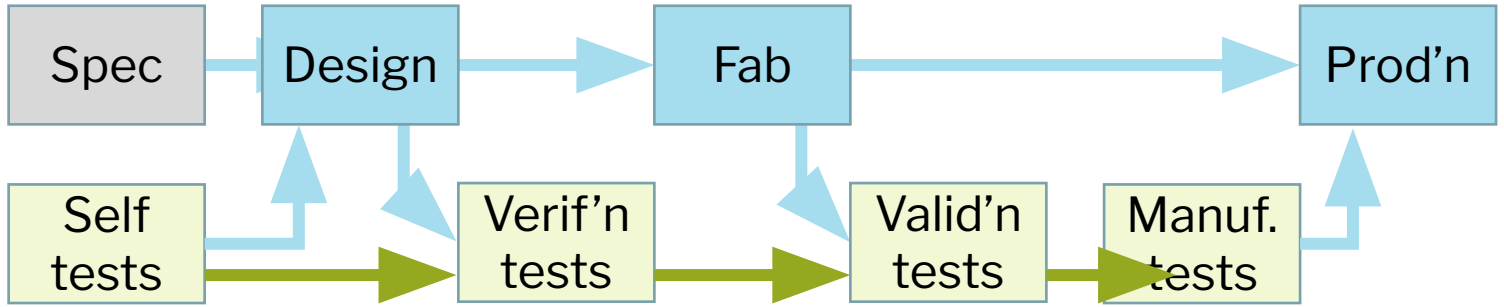
Searching for any tests that cannot be described in analog PDL

- Can describe sync/async data, arbitrary waveforms, Period|Frequency, accurate voltage delivery via resistive paths (Force/Sense), …
- Can measure/analyze voltage|current|time, instant|samples|integral, …

Deliver IP blocks with verification, self, and manufacturing tests

- PDL with a stated spec coverage and defect/fault coverage
- May eventually be required by IP block purchasers, integrators

Conclusion



Expect IEEE 1687.2 standard in 2024

- More easily describe verification and structural tests
- Automatically convert block-level tests to chip level, and to executable code
- **Reduce** time to write verification tests, and activate DfV circuitry
- **Reuse** (some) verification tests and DfV for validation and manufacturing test
- **Re-cyclize** timing for emulator, benchtop test, manufacturing test, diagnosis

Software available to convert PDL to SPICE testbench [Sunter *et al.*, ETS'23]

- Verify analog specs and manufacturing tests (incl. conditional branching)